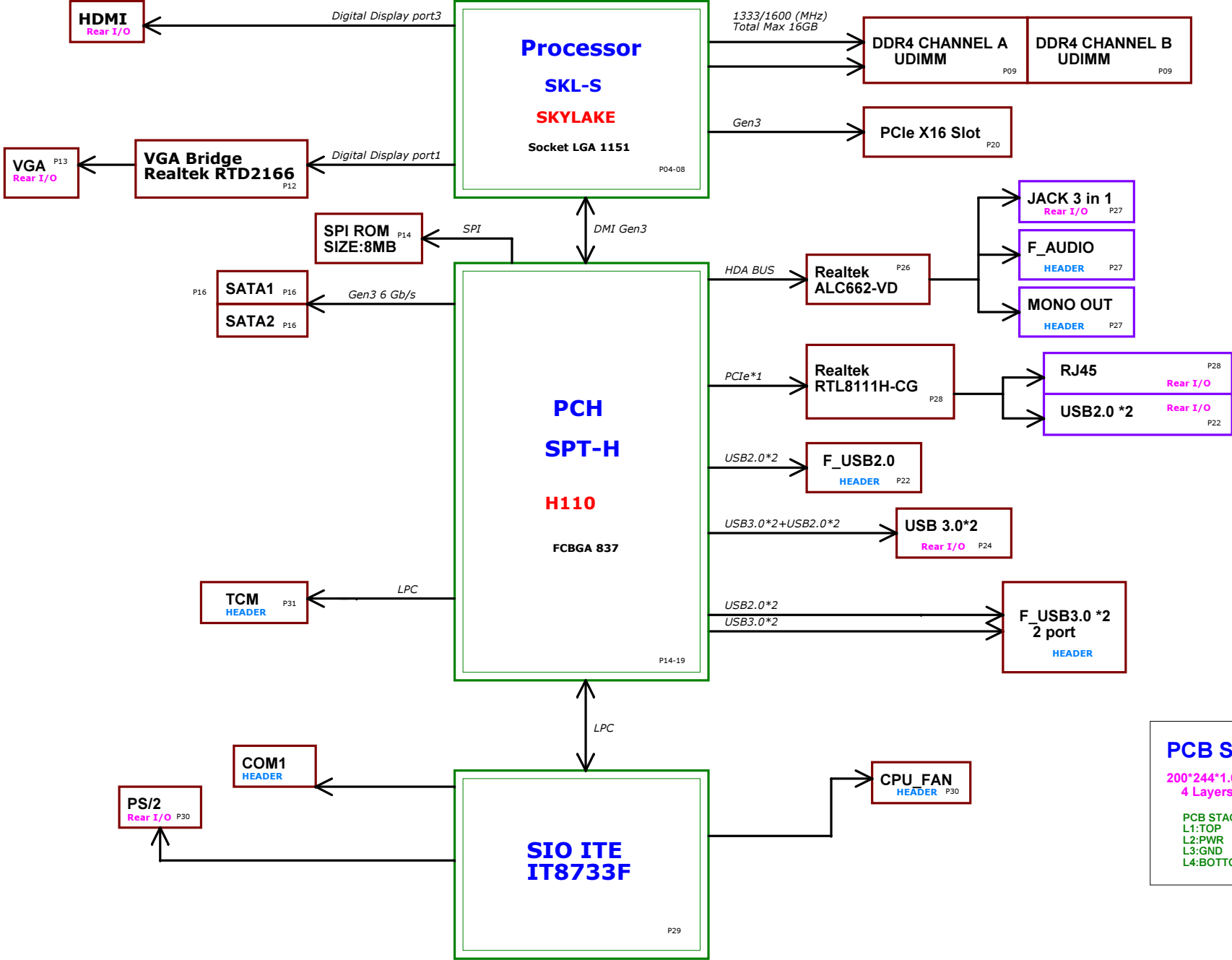


Skylake-S Desktop Platform



PCB SIZE

200*244*1.6mm
4 Layers

PCB STACK:
L1:TOP
L2:PW/R
L3:GND
L4:BOTTOM

PCH-GPIO function

Pin Name	Power Well	Usage	Default Status	
GPP_F17	3VSB	LPC_PME_L	PME#	GPI
GPD10	ATX_3VSB	GPD10 (GPD10_DIS_ME)	GPD10	OUTPUT Low/Normal, High/ME disable
GPP_B13	N/A	PCH_PLTRST_L	PLTRST#	
GPP_G15	VCC3	GPP_G15 (TMP Header Sel)	GPI	
GPP_G13	VCC3	HDPANEL_DETECT	GPI	
GPP_E7	VCC3	THERMAL_SD	GPI	
GPP_H18	3VSB	GPP_H18(BOM Detect)	GPI	
GPP_H17	3VSB	GPP_H17(BOM Detect)	GPI	
GPP_H16	3VSB	GPP_H16(BOM Detect)	GPI	
GPP_B14	+VCC3	PCH_SPKR	SPKR	
GPP_A14	3VSB	LPCPD_L	SUS_STAT#	
GPP_C6	3VSB	SML1_CLK	SML1CLK	
GPP_C7	3VSB	SML1_DATA	SML1DATA	
GPP_E8	VCC3	SATALED_L	SATALED#	
GPP_E9	3VSB	GPP_E9 (BIOS WP)	GPI	INPUT Low/Normal, High/BIOS WP
GPP_E10	3VSB	GPP_E10 (SW BIOS WP)	GPO	OUTPUT Low/BIOS WP, High/Normal
GPP_F22	VCC3	PCH_GPP_F22 (PCIEX16RST)	GPO	S0:High S3/S4/S5:Low
GPP_F16	3VSB	GPP_F16 (USB_EN)	GPO	S0/S3:High S4/S5:Low
GPP_F14	3VSB	H_SKTOCC_L	GPI	
GPD0	DSW	RLAN_PWR_EN	GPO	
GPP_D4	3VSB	SIO_GP16(PC_health)	GPI	

SIO-GPIO function

Pin Name	Power Well	Usage	Default Status
GP37	+DIMM_5VDUAL	SIO_LED1	FAN_TAC3(DI)
GP36	3VSB	THERMAL_SD	FAN_CTL3(DOD8)
GP35	+DIMM_5VDUAL	SIO_LED0	FAN_TAC4(DI)
GP34	3VSB	SUSWARN_L	SUSWARN#(DOD8)
GP33	3VSB	SUSACK_L	SUSACK#(DOD8)
GP32	ATX3VSB	DPWROK	DPWROK(DOD8)
GP30	VCC	ATX_PWRGD	ATXPG(DI)
GP14	3VSB	SML1_CLK	VCORE_EN(DOD8)
N/A	3VSB	SML1_DATA	PCH_D1
GP13	VCC3	PCH_SYSPWROK	PWROK1(DOD8)
GP12	N/A	PCIRST1_L	PCIRST1#(DO8)
GP11	N/A	PCIRST2_L	PCIRST2#(DO8)
GP44	3VSB	SIO_PWRON_L	PWRON#(DOD8)
GP54	3VSB	LPC_PME_L	PME#(DOD8)
GP43	ATX5VSB	FP_PWRBTN_L	PANSWH#(DI)
GP42	ATX3VSB	ATX_PSON_L	PSON#(DOD8)
GP53	N/A	SLP_S4_L	SUSC#(DI)
GP40	3VSB	3VBSBW_L	3VBSBW#(DO8)
GP55	3VSB	RSMRST_L	RSMRST3#(DOD8)
GP16	3VSB	SIO_GP16(PC_health)	5VSB_CTRL3#(DOD8)

Interrupt mapping

Data:2016/06/16

Function	INT# port	PCle*1 port	Device
LAN	INTB#	Port 6	RTL8111H
SATA	INTA#	NA	SATA3.0

CPU&PCH-Strap

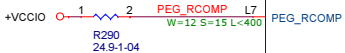
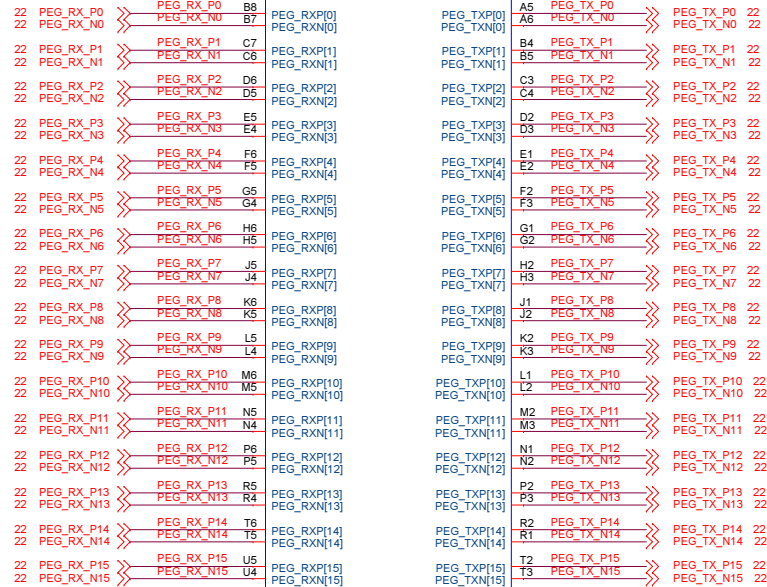
Pin Name	Usage	Default Status
CFG0	CFG[0]: Stall reset sequence after PCU PLL lock until de-asserted	1 = (Default) Normal Operation
CFG1	CFG[1]: Reserved configuration lane	
CFG2:5:6	CFG[2]:1 = Normal operation CFG[6:5]:11 = 1 x16 PCI Express	PCIE16X
CFG3	CFG[3]: Reserved configuration lane.	
CFG4	CFG[4]: eDP enable:	1 = Disabled.
CFG7	CFG[7]: PEG Training:	1 = (default) PEG Train immediately following RESET# de assertion.
CFG19:8	CFG[19:8]:Reserved configuration lanes.	
SPKR/GPP_B14	Top Swap Override	0 =Disable "Top Swap" mode. (Default)
GSPI0_MOSI/GPP_B18	No Reboot	0 =Disable "No Reboot" mode
SMBALERT#/GPP_C2	TLS Confidentiality	1 =EnableIntel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS
GSPI1_MOSI/GPP_B22	Boot BIOS Strap Bit BBS	0=SPI
SML0ALERT#/GPP_C5	eSPI or LFC	0 =LFCIs selected for EC.
HDA_SDO	Flash Descriptor Security Override	This signal has a weak internal pull-down. 0 =Enable security measures defined in the Flash Descriptor. 1 =Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.
DDPB_CTRLDATA/GPP_I6	Display Port B Detected	1 = Port B is detected.
DDPC_CTRLDATA/GPP_I8	Display Port C Detected	1 = Port C is detected.
DDPB_CTRLDATA/GPP_I10	Display Port D Detected	1 = Port D is detected.

20160728 Derek
CPU1->CPU for silk request.

CPUC

SKT_H4?

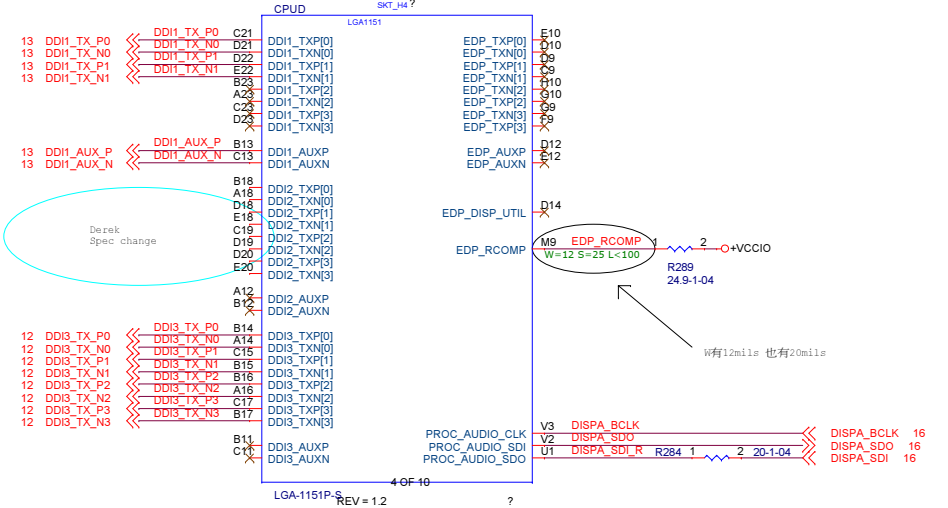
LGA1151

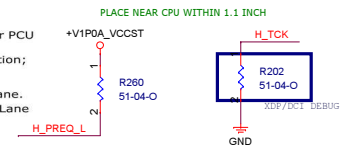


LGA-1151P-S
REV = 1.2

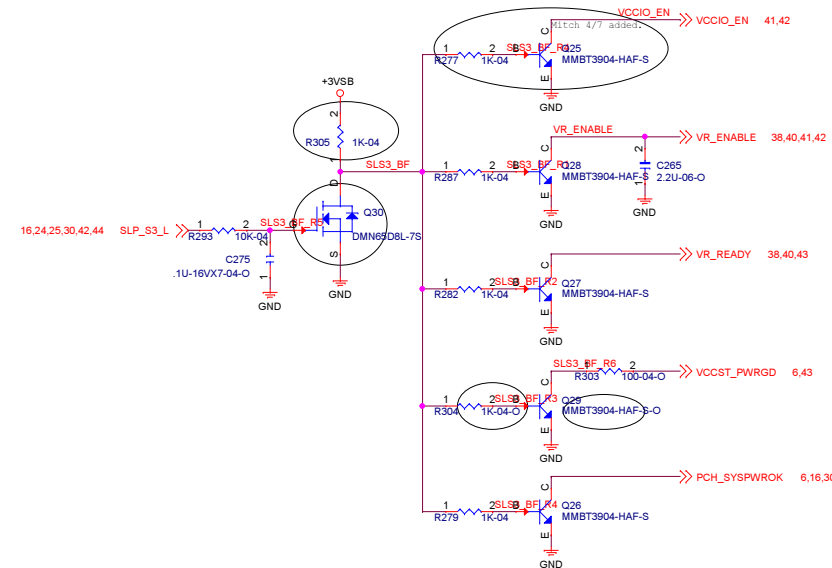
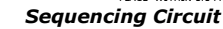
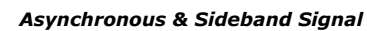
DP to VGA

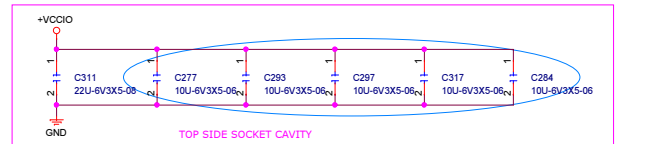
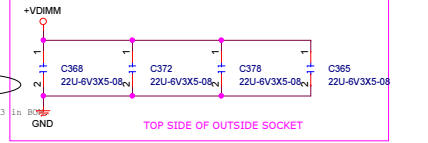
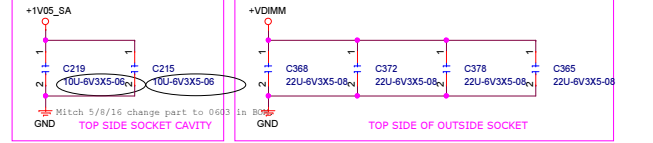
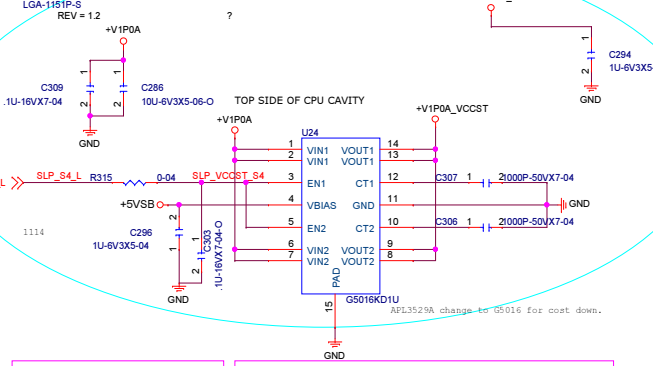
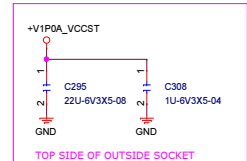
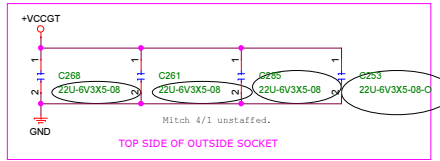
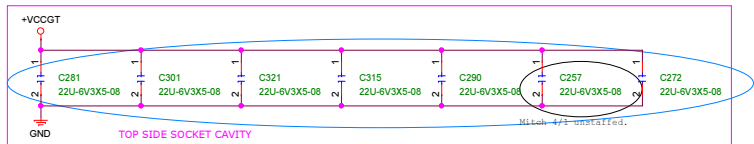
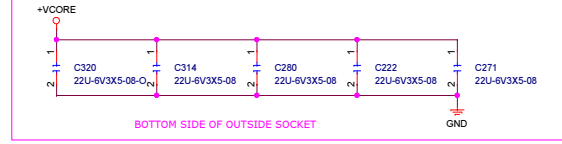
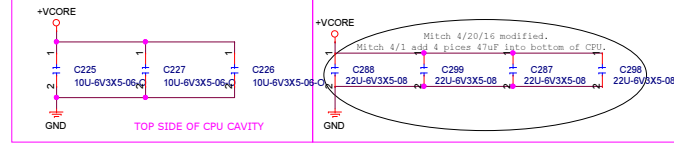
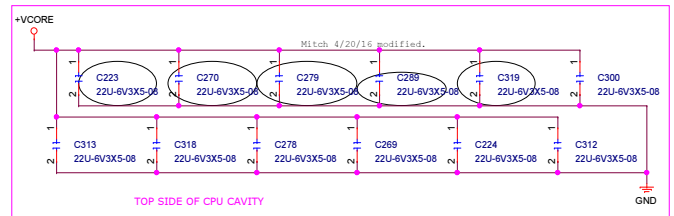
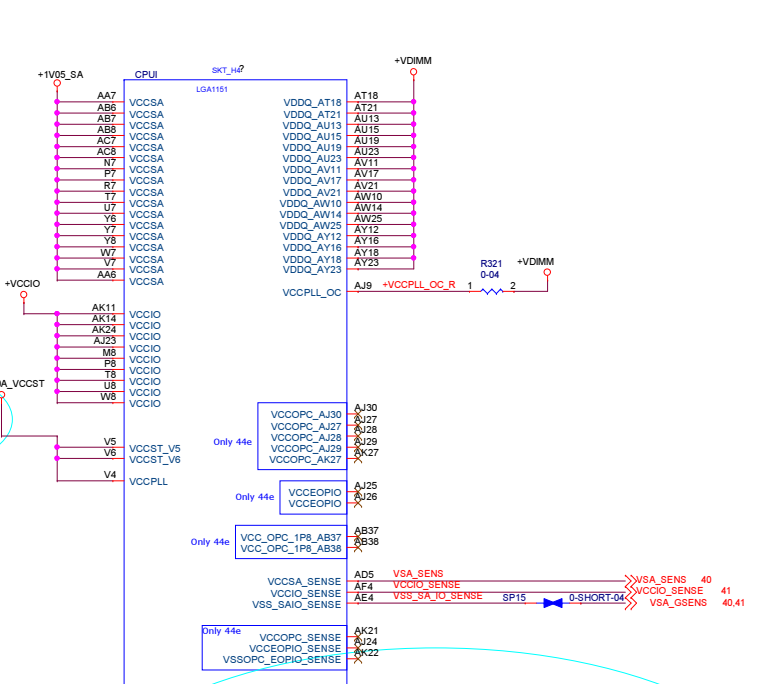
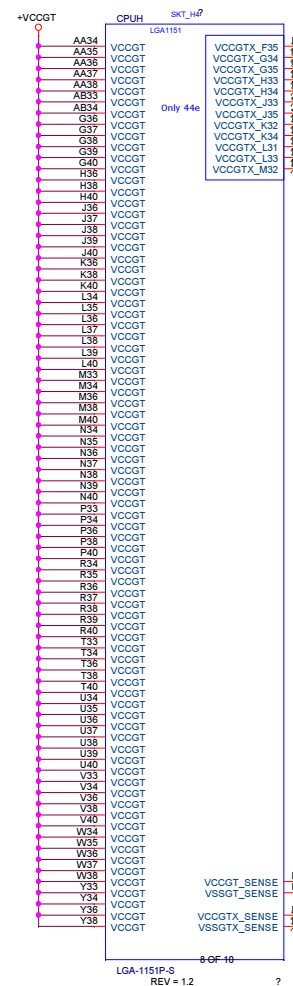
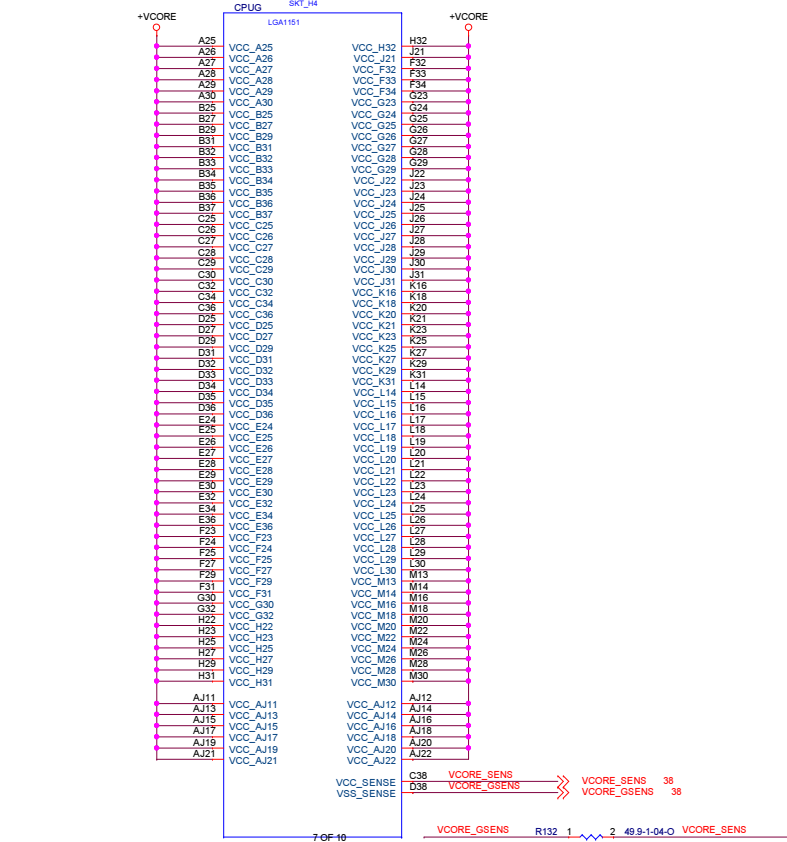
HDMI

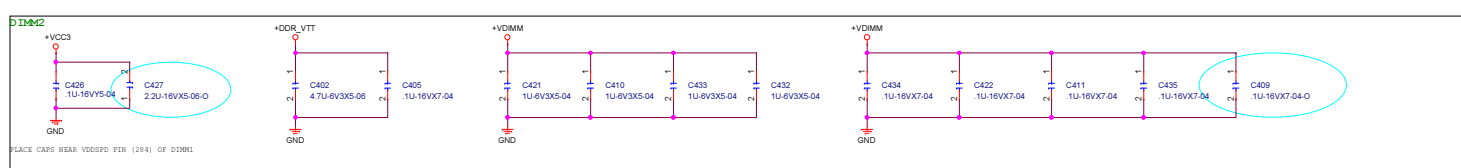




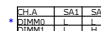
- **CFG[0]:** Stall reset sequence after PCI PLK lock until de-asserted;
 - 1 = (Default) Normal Operation;
 - 0 = Stall.
- **CFG[1]:** Reserved configuration lane.
- **CFG[2]:** PCI Express* Static x16 Lane Numbering Reversal.
 - 1 = Normal operation
 - 0 = Lane numbers reversed.
- **CFG[3]:** Reserved configuration lane.
- **CFG[4]:** eDP enable;
 - 1 = Disabled.
 - 0 = Enabled.
- **CFG[6:5]:** PCI Express* Bifurcation
 - 00 = 1 x8, 2 x4 PCI Express*
 - 01 = reserved
 - 10 = 2 x8 PCI Express*
 - 11 = 1 x16 PCI Express*
- **CFG[7]:** PEG Training
 - 1 = (default) PEG Train immediately following RESET# de-assertion.
 - 0 = PEG Wait for BIOS for training.
- **CFG[19:8]:** Reserved configuration lanes.



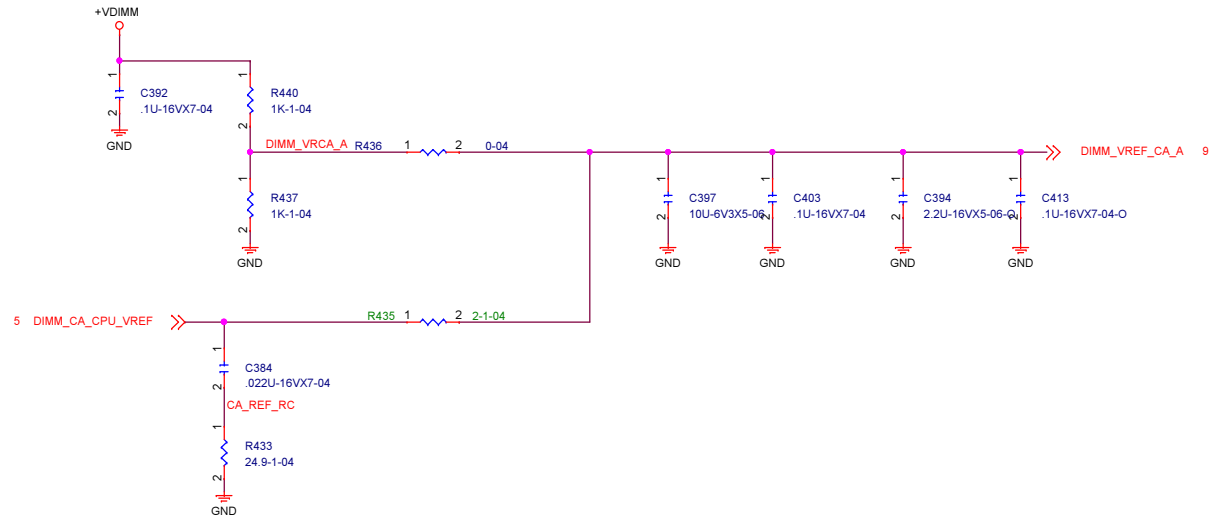




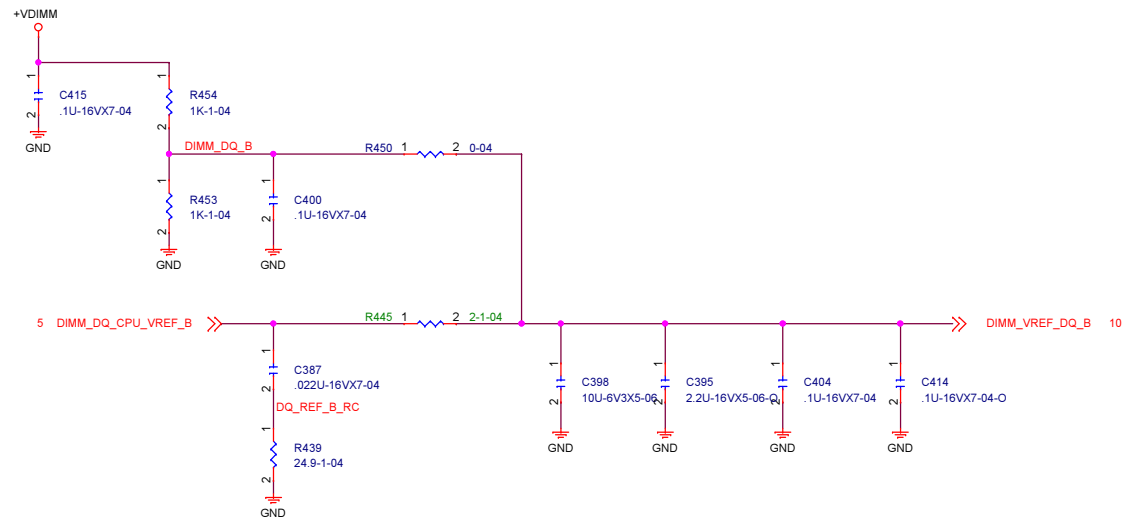
5	M_DQS_A_P8	M_DQS_A_P8
5	M_DQS_A_N8	M_DQS_A_N8
5	M_MA_A16	M_MA_A16
5	M_BG_A0	M_BG_A0
5	M_BG_A1	M_BG_A1
5	M_DATA_A_C85	M_DATA_A_C85
5	M_DATA_A_C84	M_DATA_A_C84
5	M_DATA_A_C80	M_DATA_A_C80
5	M_DATA_A_C83	M_DATA_A_C83
5	M_DATA_A_C82	M_DATA_A_C82
5	M_DATA_A_C81	M_DATA_A_C81
5	M_DATA_A_C86	M_DATA_A_C86
5	M_DATA_A_C87	M_DATA_A_C87
5	M_ACT_A_L	M_ACT_A_L
5	M_PARITY_A	M_PARITY_A
5	M_ALERT_A_L	M_ALERT_A_L



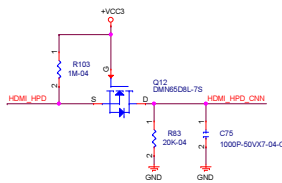
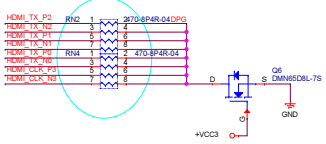
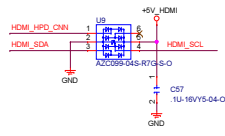
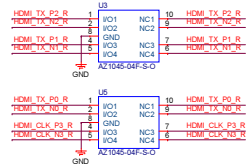
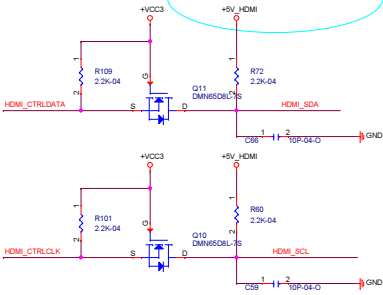
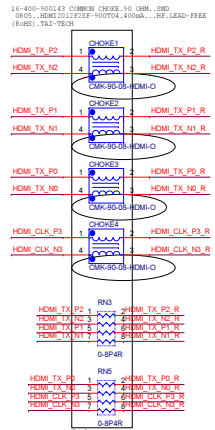
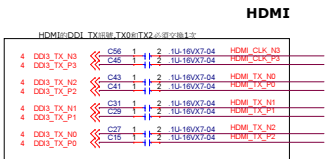
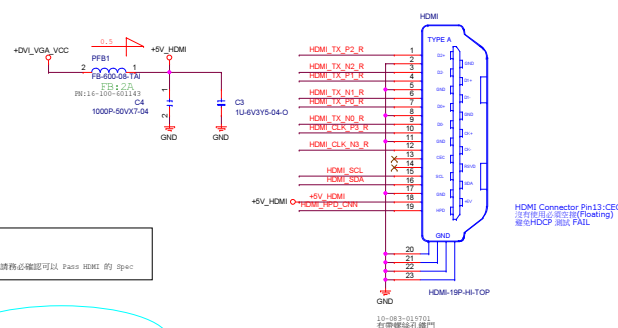
DIMM_VREF_CA



DIMM_VREF_DQ

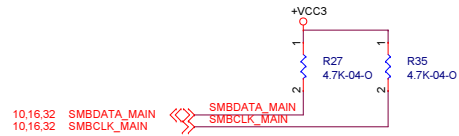
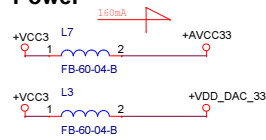


Port 2	DOI2_THP[0]	DOI2_LANE0_DP	HDMIx_TX2_DP
	DOI2_THP[0]	DOI2_LANE0_DN	HDMIx_TX2_DN
	DOI2_THP[1]	DOI2_LANE1_DP	HDMIx_TX1_DP
	DOI2_THP[1]	DOI2_LANE1_DN	HDMIx_TX1_DN
	DOI2_THP[2]	DOI2_LANE2_DP	HDMIx_TX0_DP
	DOI2_THP[2]	DOI2_LANE2_DN	HDMIx_TX0_DN
	DOI2_THP[3]	DOI2_LANE3_DP	HDMIx_CLK_DP
	DOI2_THP[3]	DOI2_LANE3_DN	HDMIx_CLK_DN



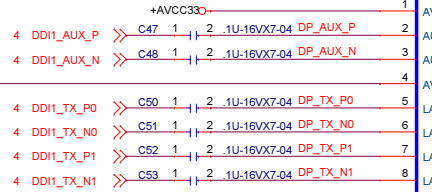
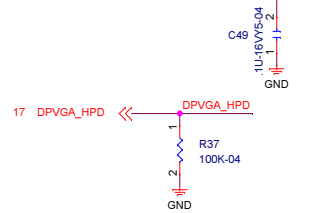
Derek
Spec change

Power



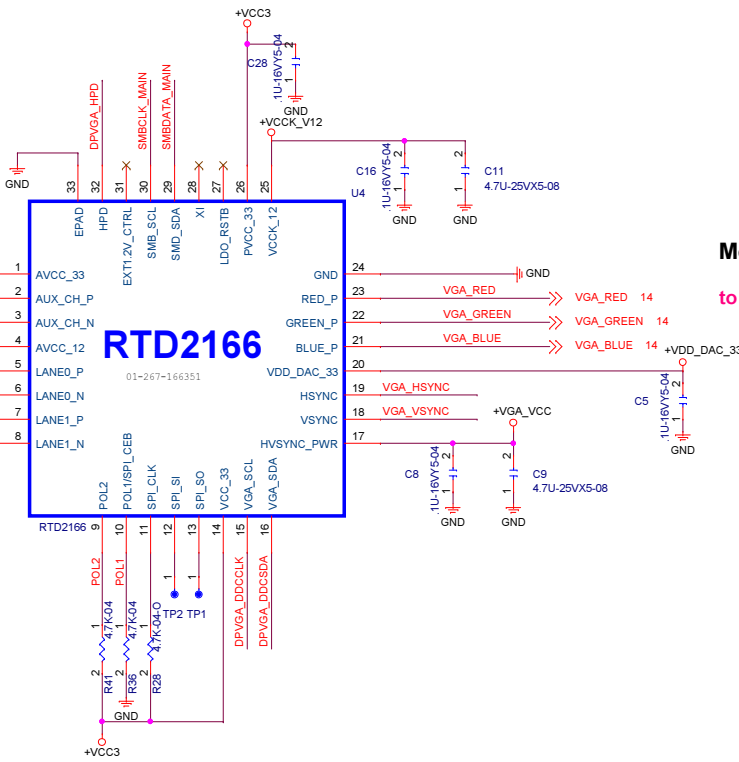
IIC Protocol is used

RTD2168 Slave Address:
0x64/0x65 and 0x68/0x69



RTD2166

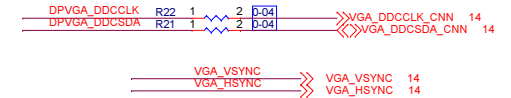
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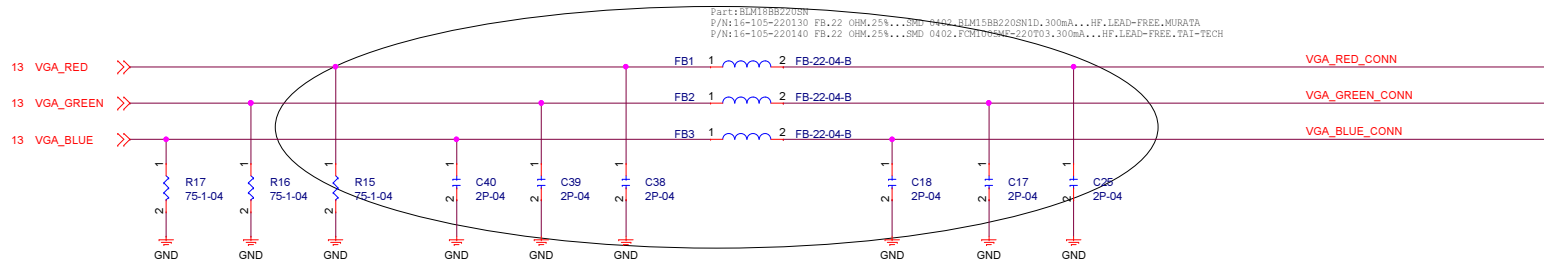
Mode Configure Table(Power On Latch)

to set PIN22 pull low, PIN23 pull high for Rom mode.

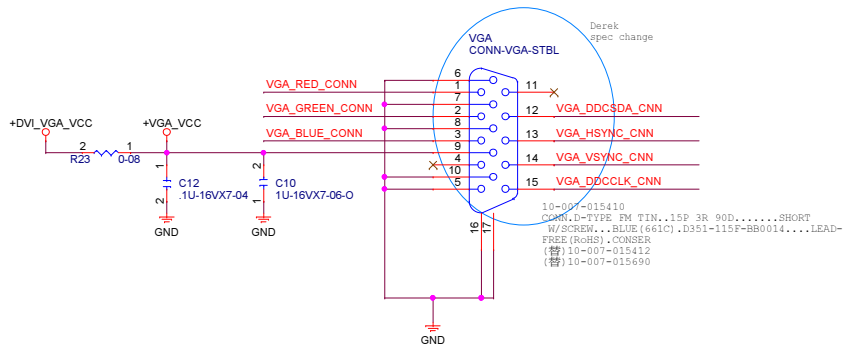
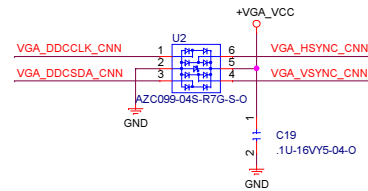
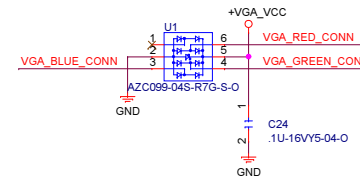
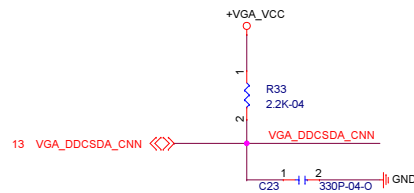
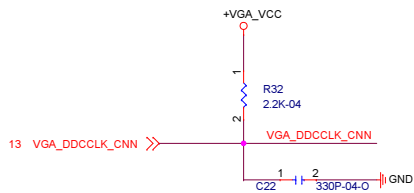
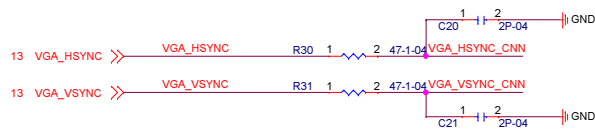
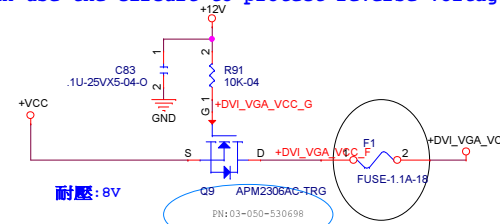
20160804 Derek
R21 ~ R22 33->0 ohm for SI test.

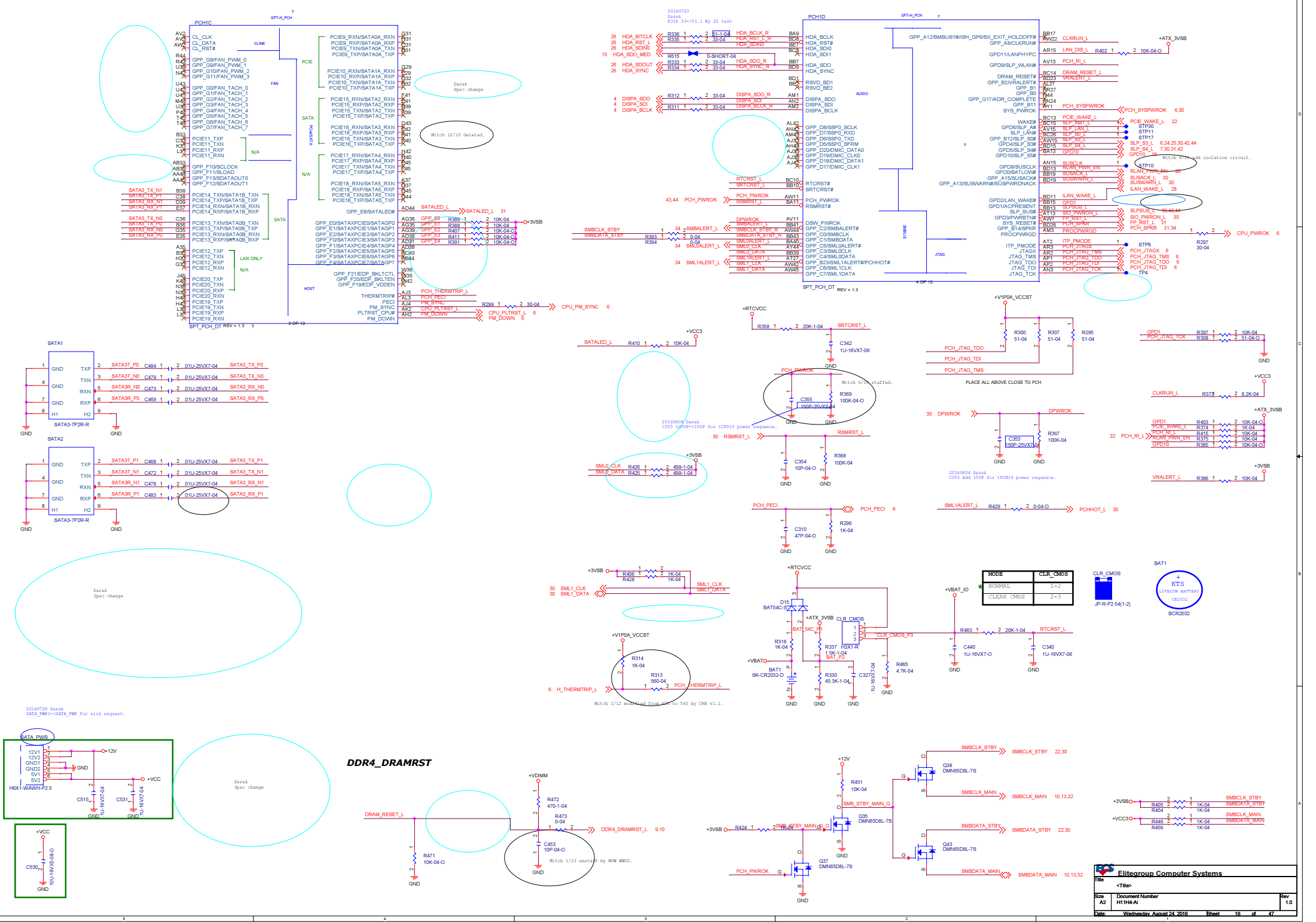


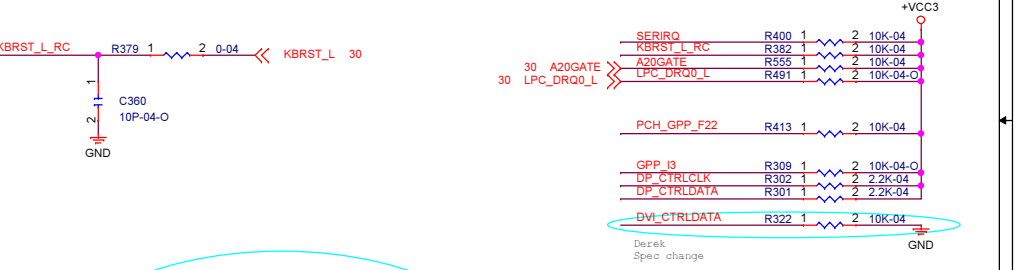
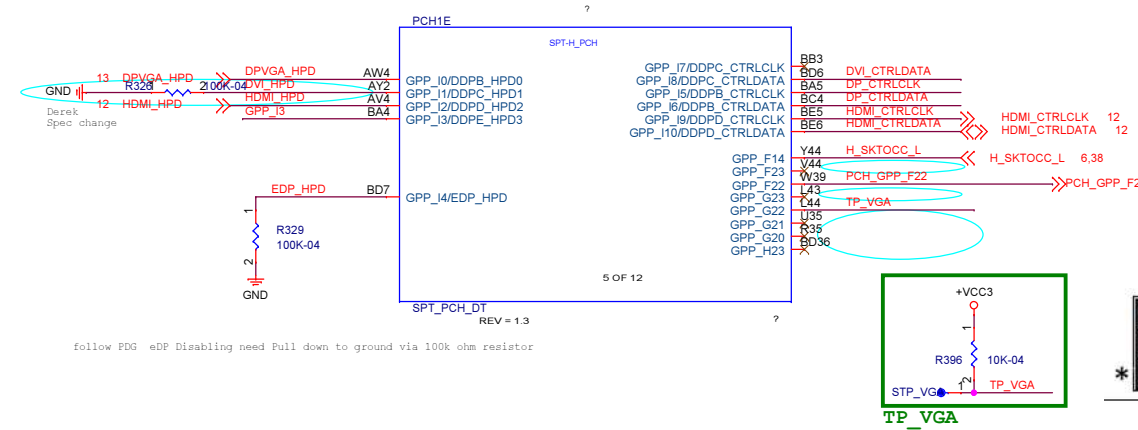
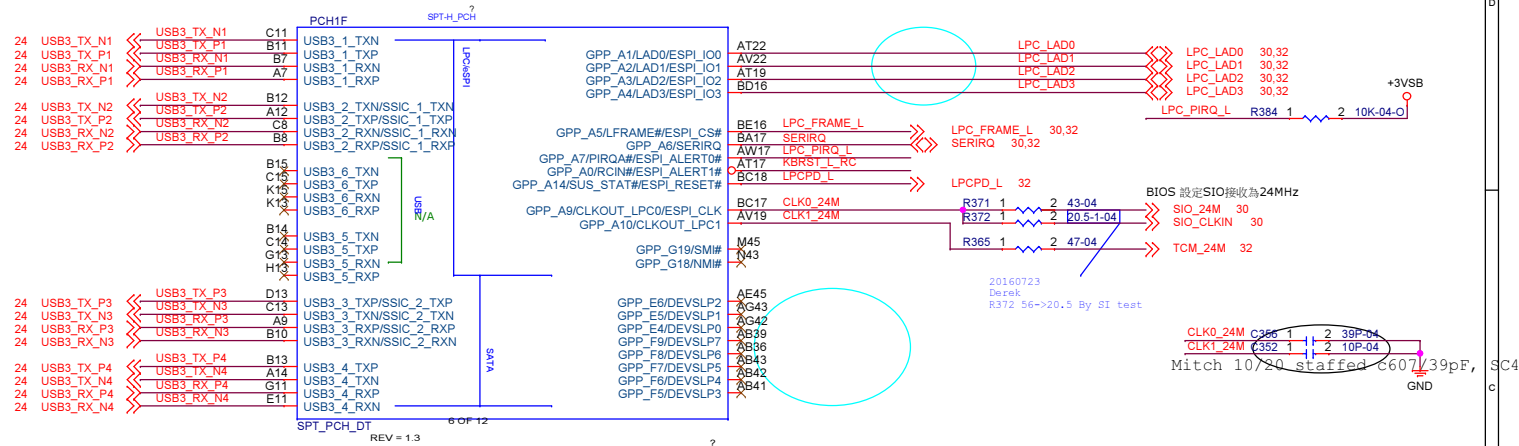
VGA



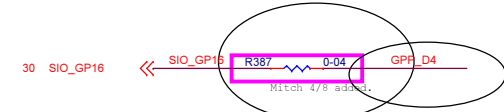
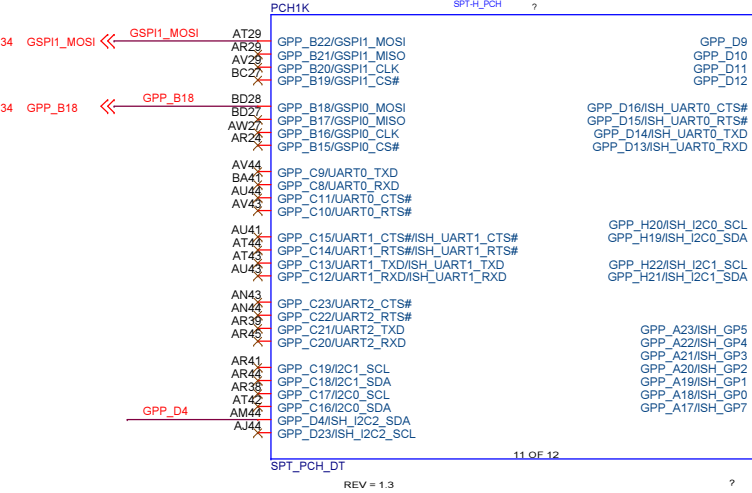
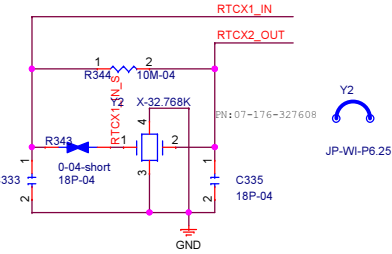
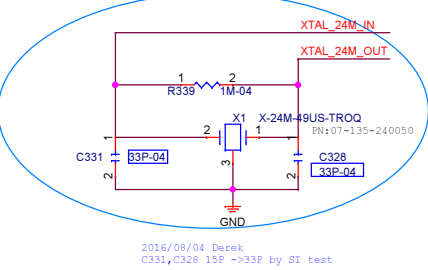
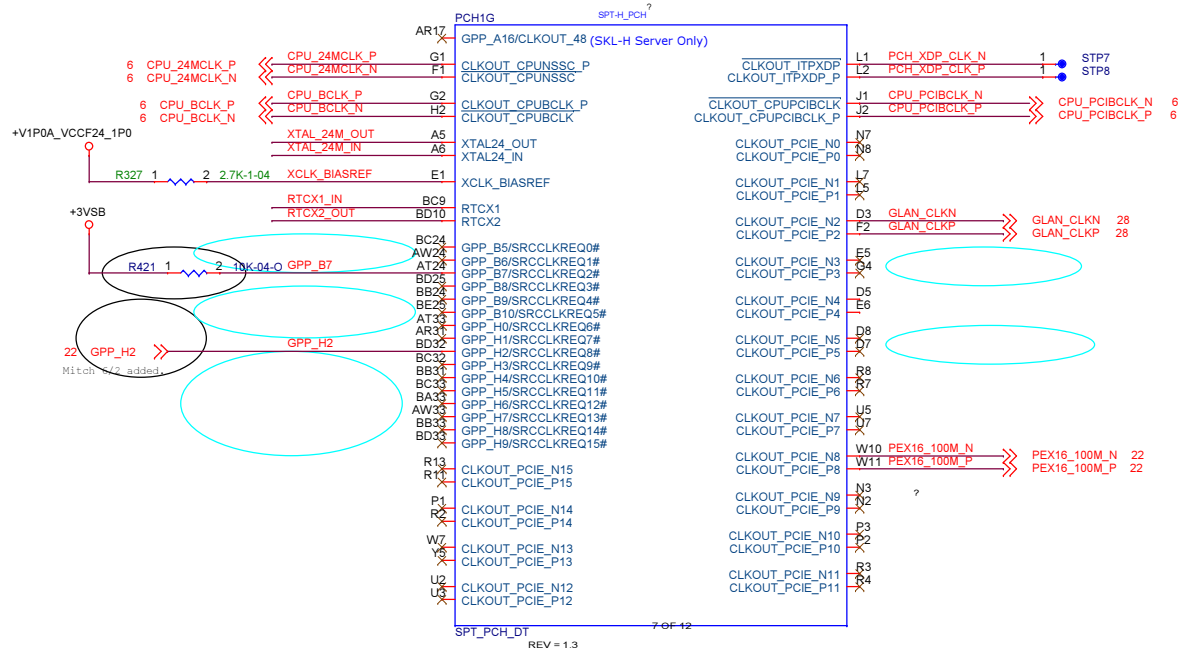
If build in Internal DVI Con,
that can use the circuit to protect reverse voltage together.

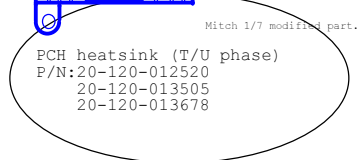
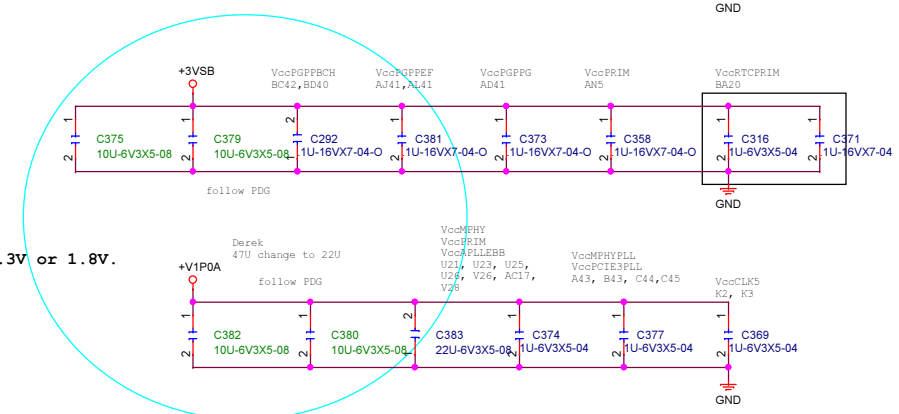
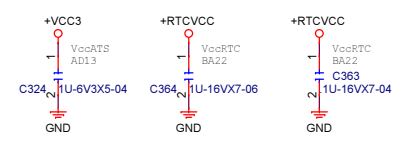


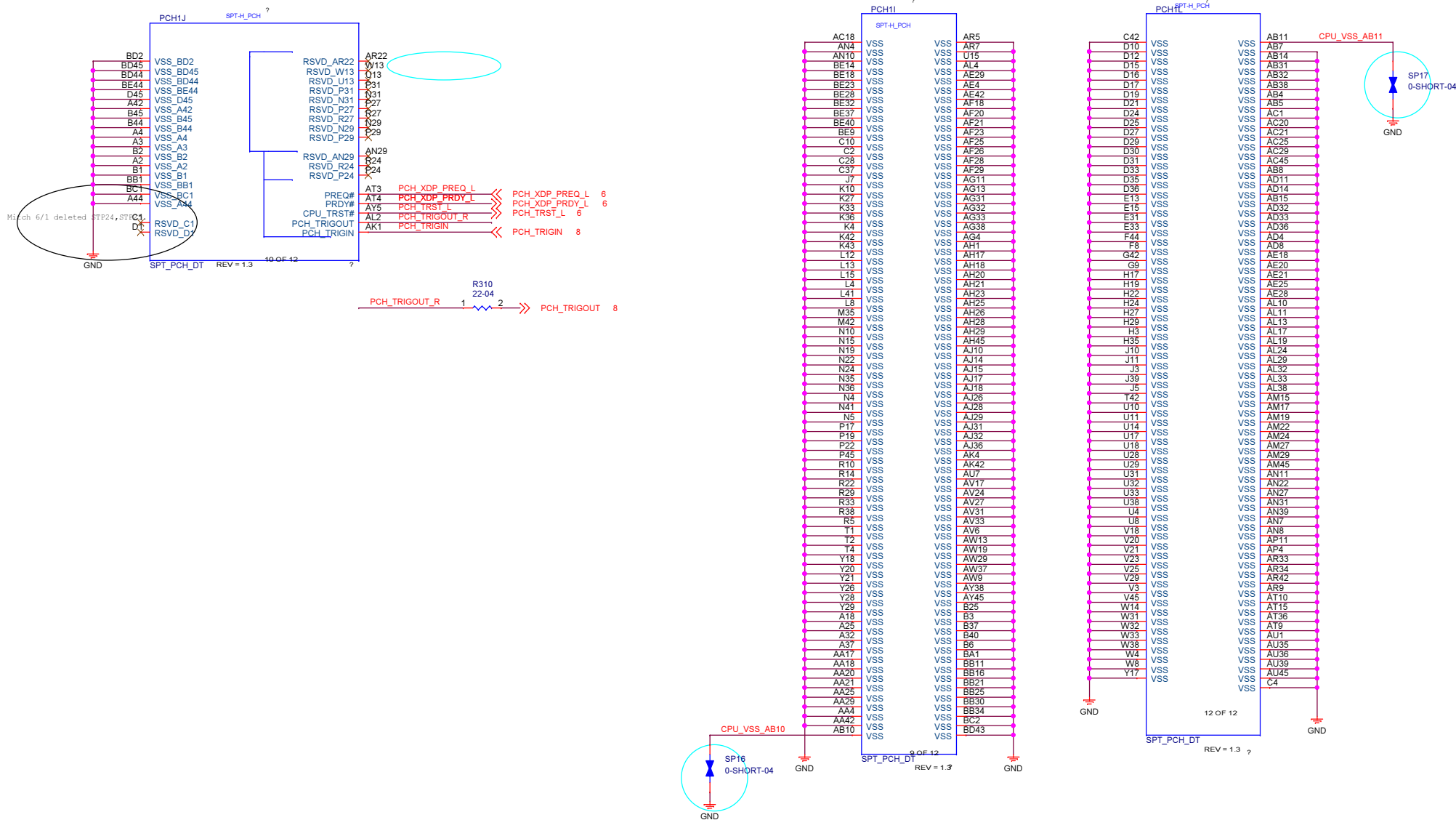




GPIXX	Display Type
Low	onboard VGA
* High	default BIOS







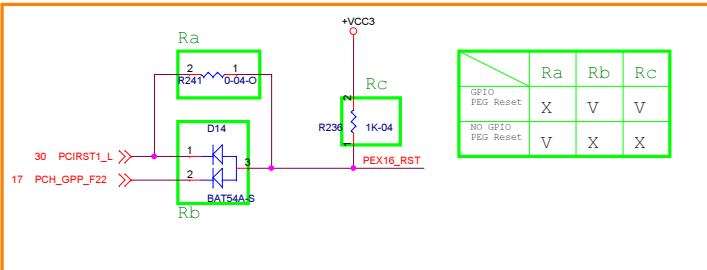
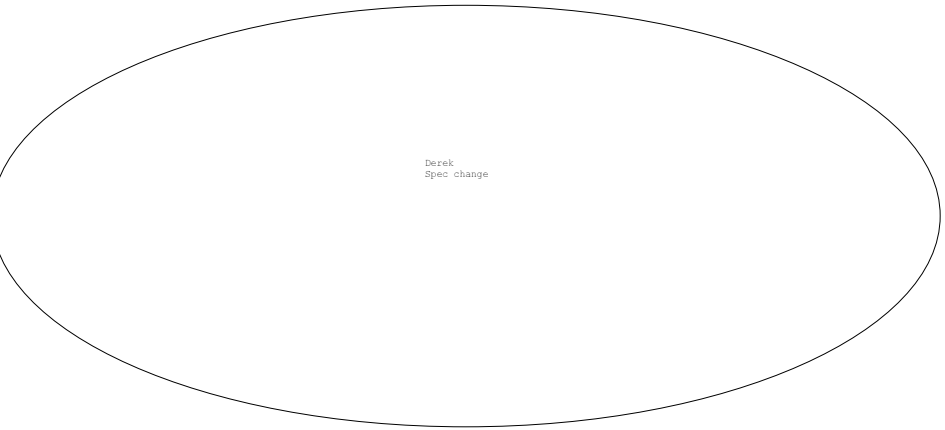
PCI-E X16 SLOT

****PCI-E SPEC****
VCC3:3A
12V:5.5A
3VSB:0.375A

PCI-E X1 SLOT1

Mitch 2/3 modified.

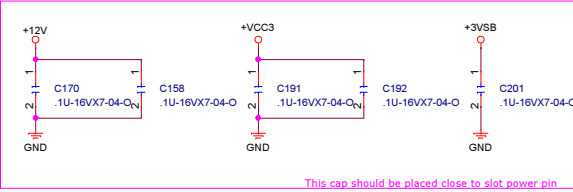
one slot support dual lan card, reserve



	Ra	Rb	Rc
GPIO PEG Reset	X	V	V
NO GPIO PEG Reset	V	X	X



Between PCI-E X16 Slot & PCI-E X1 Slot



This cap should be placed close to slot power pin

D

5

c

c

8

2

A

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Document Number

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1.0

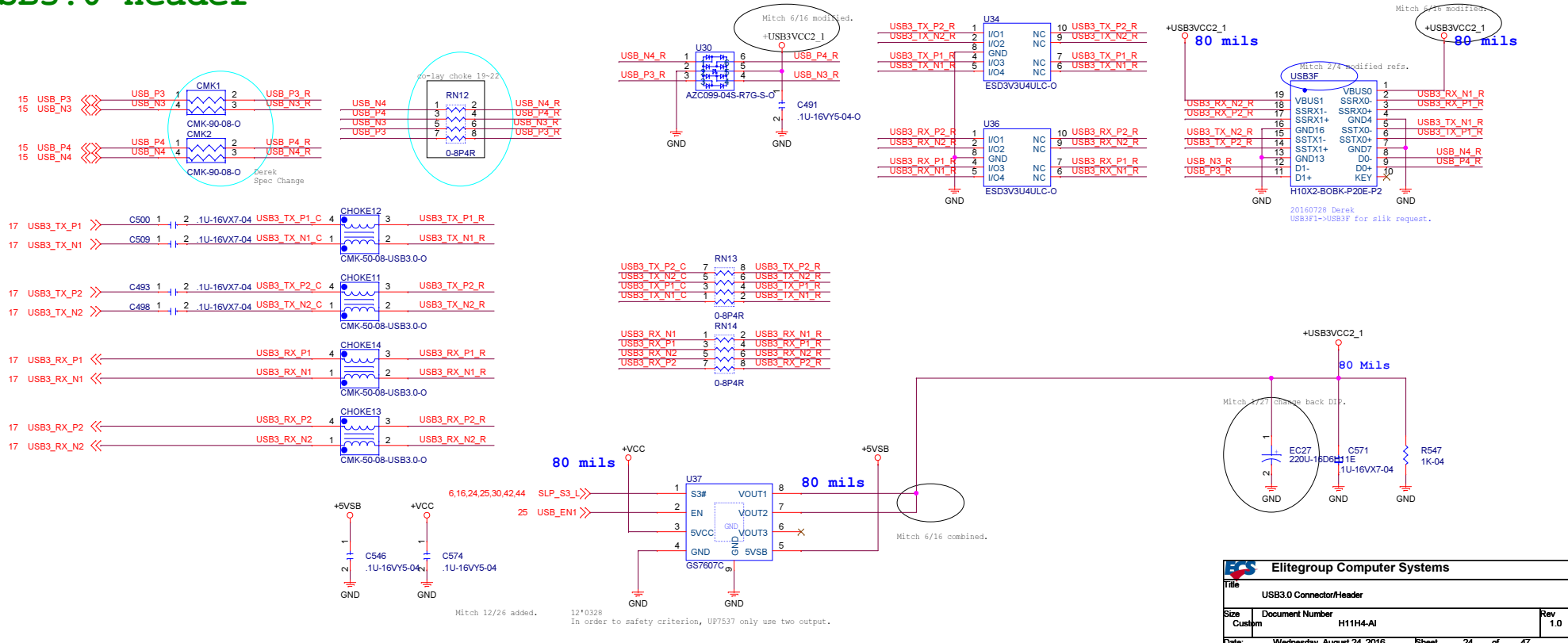
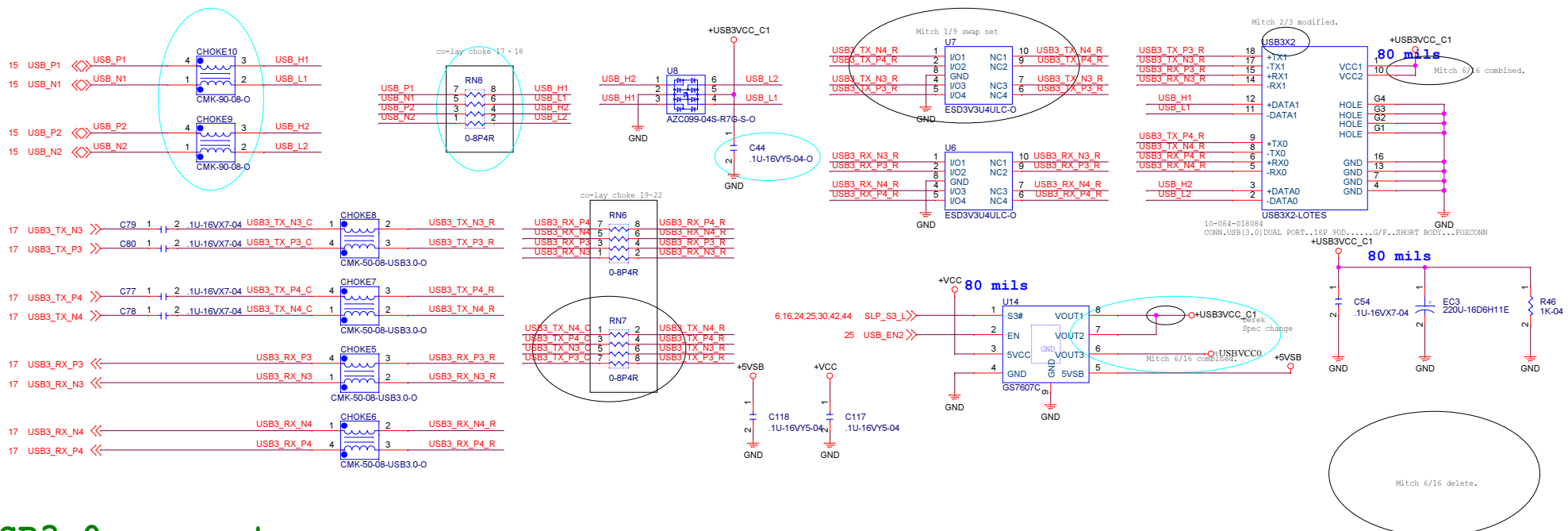
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Wednesday, August 24, 2011

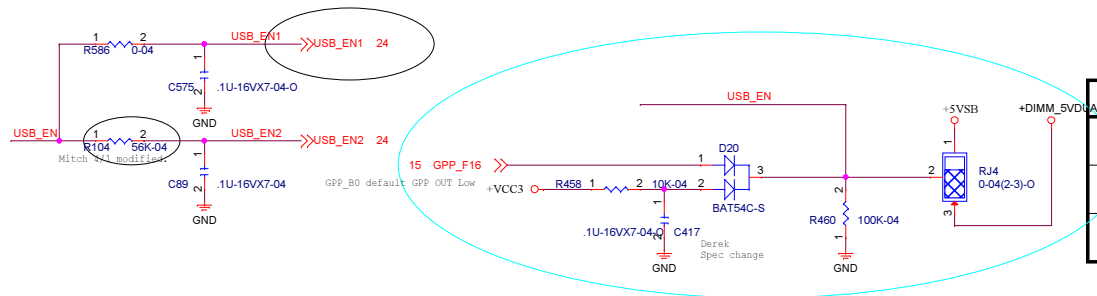
Sheet

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USB3.0 connector USB3.0 Header

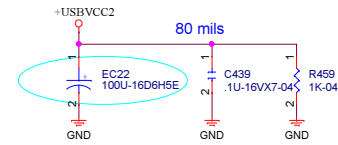
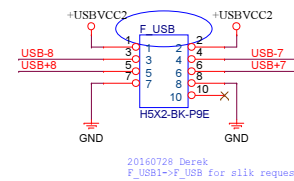
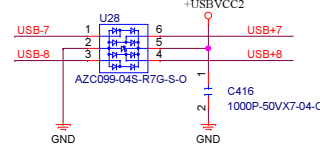
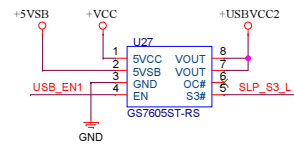
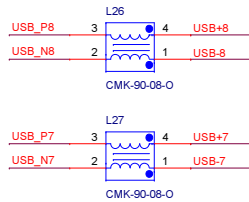
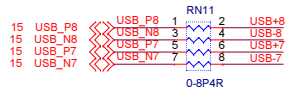


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Title			
USB3.0 Connector/Header			
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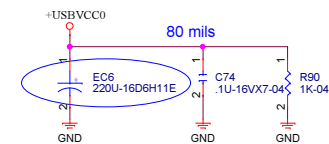
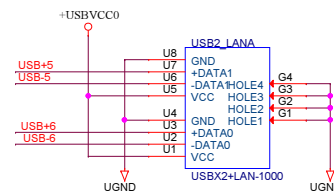
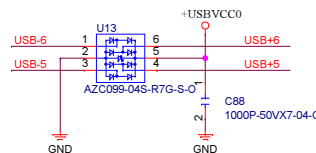
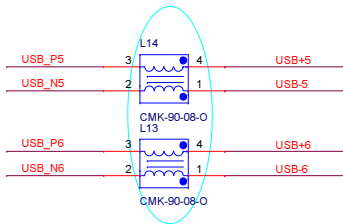
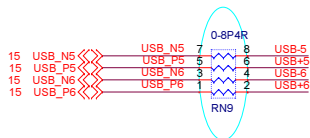
uP7536 Enable use	RJ?	RJ?	S4/S5 USB_5V_DUAL	Customer
VDIMM	0ohm (1-2)	NA	0 Volt	Acer S4 w/o S5 w/ USB_5VDUAL
5VSB	0ohm (2-3)	NA	5 Volt	
* GPIO	NA	0 ohm	S4 : 0 Volt S5 : 5 Volt	

6,16,24,30,42,44 SLP_S3_L SLP_S3_L



USB2.0 header

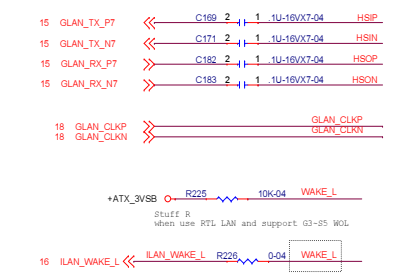
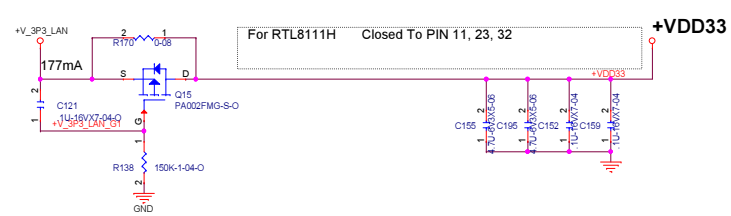
USB2.0 connector



Lan + USB2.0

10-084-022312 LAN Surge
10-084-022256 No-Surge

Elitegroup Computer Systems			
Title USB2.0 Connector/Header			
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Wake on LAN (WOL) set to ON ==> In BIOS and OS								
	LED		S0	S1	S3	S4	S5	G3 to S5 unplug and plug power cord
Rear Side	ACTIVE-LED (Single Color)	Access:Blink	Blink	Blink	Blink	Blink	Blink	OFF
		Others:OFF	OFF	OFF	OFF	OFF	OFF	OFF
	SPEED-LED (Dual Color)	Disconnected:OFF	OFF	OFF	OFF	OFF	OFF	OFF
		1000:ON with A color:Amber	Amber	OFF	OFF	OFF	OFF	OFF
		100:ON with B color:Green	Green	OFF	OFF	OFF	OFF	OFF
Front Side	(Single Color)	10:OFF	OFF	OFF	OFF	OFF	OFF	
		Access: Blinking Others: OFF	Access: Blinking Others: OFF	Access: Blinking Others: OFF	OFF	OFF	OFF	

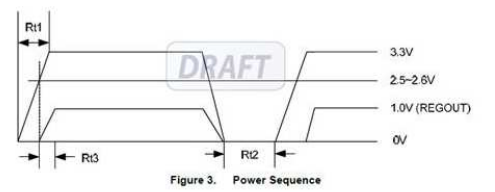
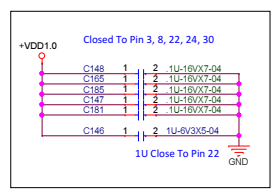
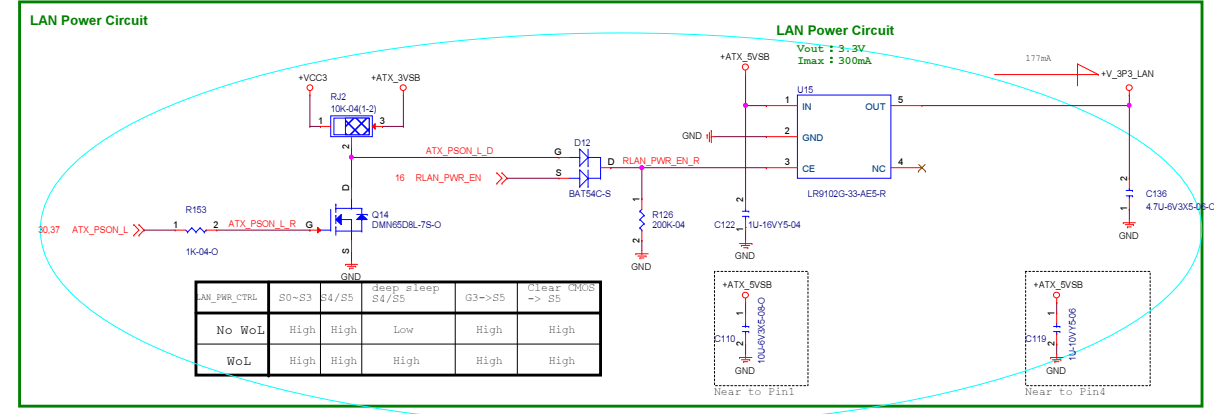
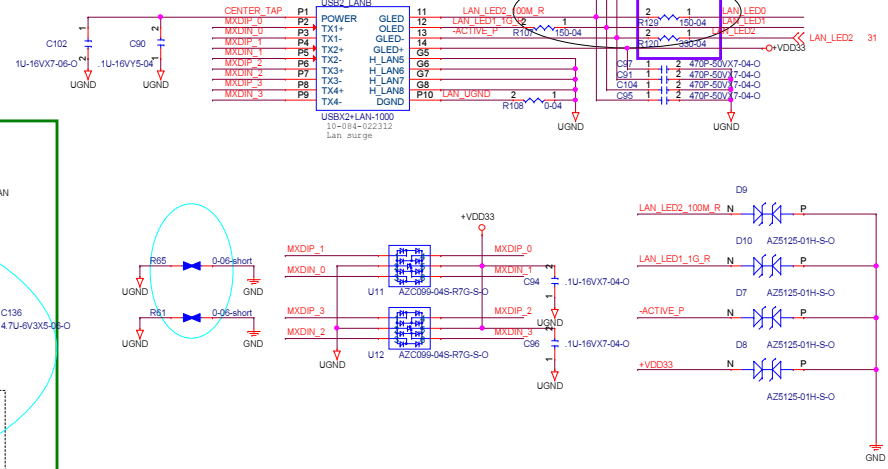
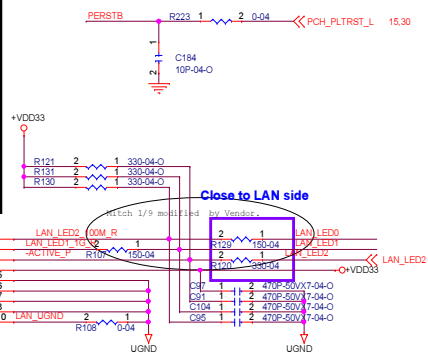
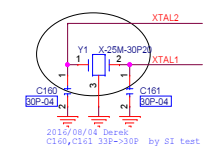
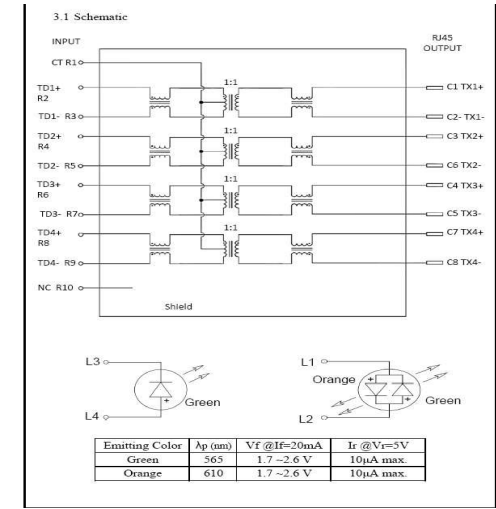
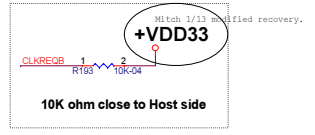



Table 24. Power Sequence Parameter

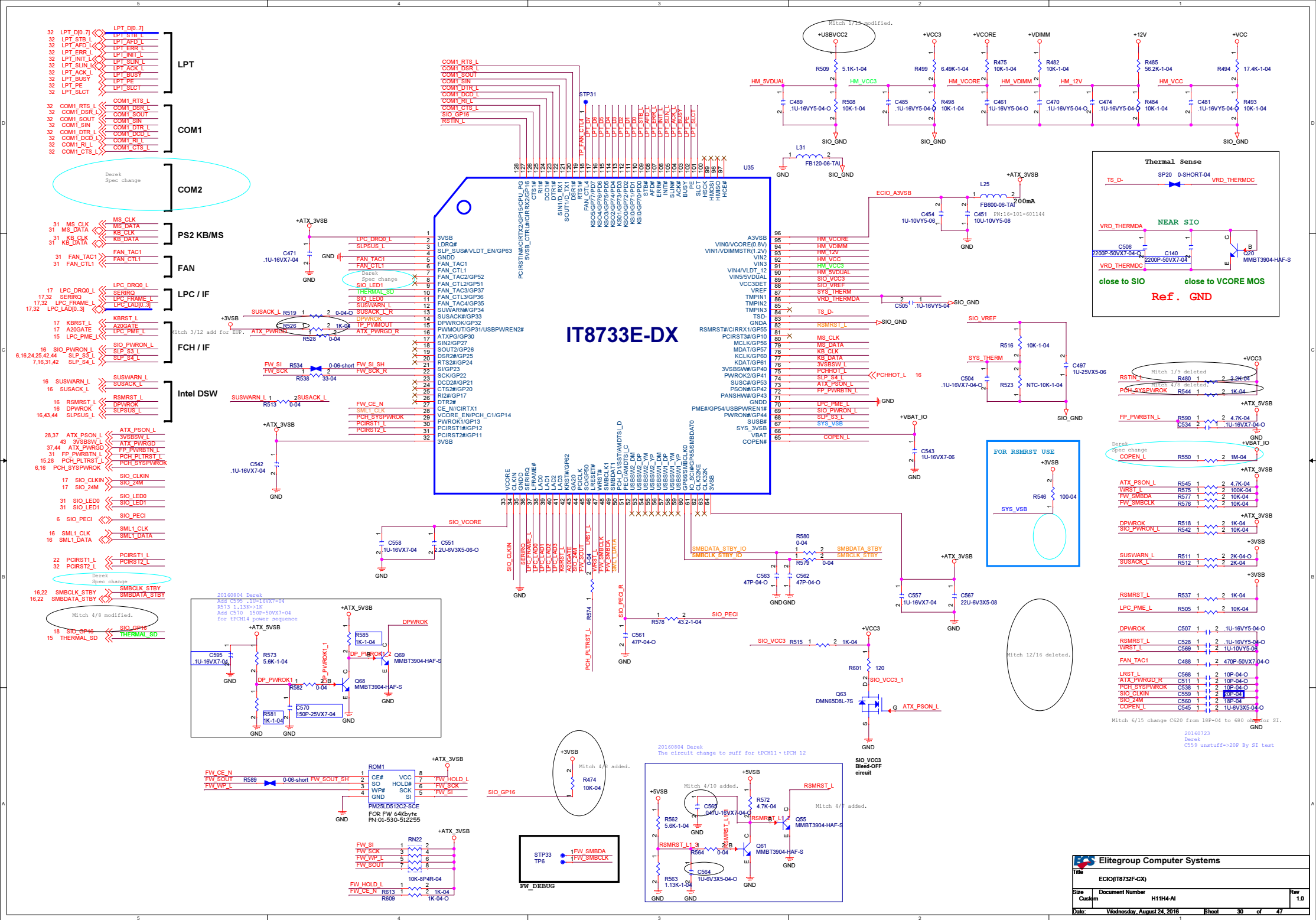
Symbol	Description	Min	Typical	Max	Units
Rt1	3.3V Rise Time	0.5	-	100	ms
Rt2	3.3V Off Time	50	-	-	ms
Rt3	1.0V (REGOUT) Settle Time	-	-	15	ms

Note: See the following section for power sequence requirements.




5		4		3		2		1
D								D
C								C
B								B
A								A
5		4		3		2		1

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Title FAN/Buzzer/PS2/Front Panel			
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18 GSP1_MOSI << 1 STP12

BOOT SELECT STRAP
IF SAMPLED HIGH, LPC IS SELECTED ELSE SPI
PCH HAS INTERNAL WEAK PD

16,31 PCH_SPKR << 1 STP28

Top Swap Override
The signal has a weak internal pull-down.
0 = Disable "Top Swap" mode. (Default)
1 = Enable "Top Swap" mode.

18 GPP_B18 << 1 STP14

NO REBOOT IF SAMPLED HIGH
PCH HAS INTERNAL WEAK PD

15 GPP_H12 << 1 STP20

ESPI FLASH SHARING MODE
PCH HAS INTERNAL WEAK PD
0: MASTER ATTACHED FLASH SHARING
1:SLAVE ATTACEHD FLASH SHARING

15 USB_OC3_L << 1 STP24

DFX TEST MODE
XTAL INPUT IS SINGLE ENDED IF SAMPLED LOW ELSE DIFFERENTIAL

16 SML0ALERT_K << 1 STP25

ESPI/LPC SELECT STRAP
IF SAMPLED HIGH, ESPI IS SELECTED ELSE LPC
PCH HAS INTERNAL WEAK PD

15,33 SPL_MOSI << R378 1 2 1K-04 +3VSB

BOOT HALT ENABLED IF LOW
PCH HAS INTERNAL WEAK PU

15,33 SPL_MISO << R381 1 2 1K-04 +3VSB

JTAG ODT IS DISABLED IF LOW
PCH HAS INTERNAL WEAK PU

15 SPI0_IO2 << 1 STP22

CONSENT STRAP IS ENABLED IF LOW
PCH HAS INTERNAL WEAK PU

15 SPI0_IO3 << 1 STP18

PESONALITY STRAP IS ENABLED IF LOW
PCH HAS INTERNAL WEAK PU
(P.S. Pull down for pre ES1/ES1 only)


Mitch 6/19 unstaffed.

16 SMBALERT_L << R427 1 2 4.7K-04 +3VSB

TLS CONFIDENTIALITY ENABLED
IF SAMPLED HIGH (DEFAULT)
PCH HAS INTERNAL WEAK PD

16 SML1ALERT_K << 1 STP13

EXI BOOT STALL BYPASS IS ENABLED IF SAMPLED HIGH
PCH HAS INTERNAL WEAK PD

			
Title Strap Pin			
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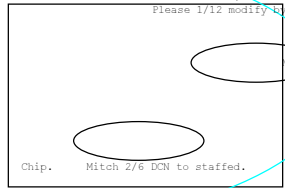
Mitch 4/15 VB unstaffed.
Mitch 1/15 modified by Intel rework mail.

Mitch 4/15 VB unstaffed.

Mitch 4/15 VB unstaffed.

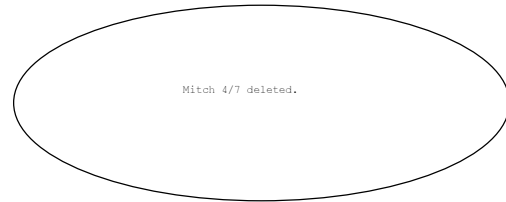
DDR_VTT Disable

Mitch 4/15 VB unstaffed.
02-342-375450
IC REG.SLG7NT4375V..STQFN 12P.....HF.LEAD-FREE.SILEGO



Mitch 4/15 VB unstaffed.
Please 1/12 modify H11H4-AM.

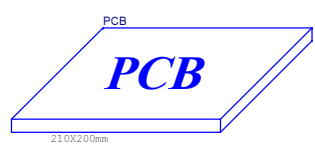
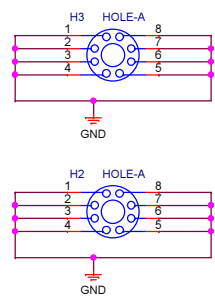
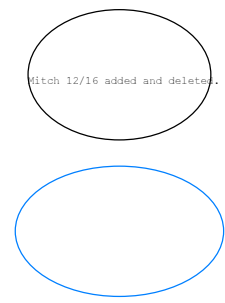
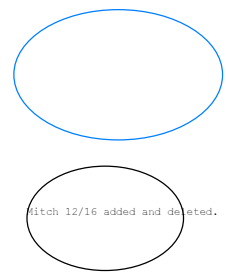
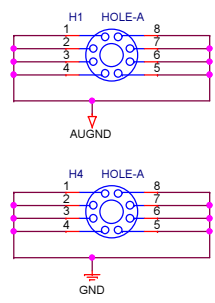
Mitch 4/8 invert VDDQ_BLEED control.



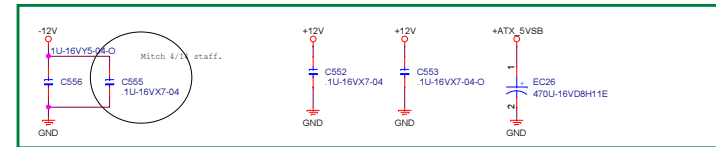
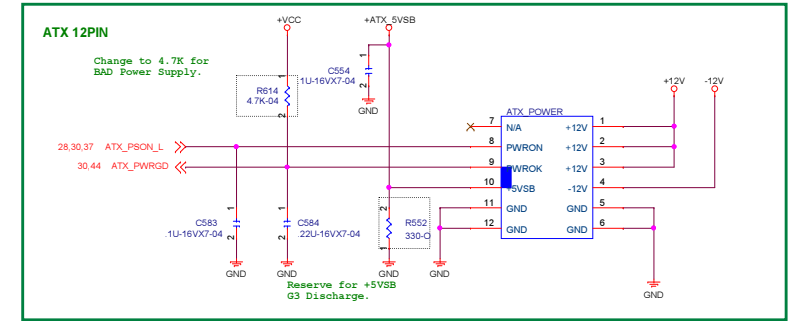
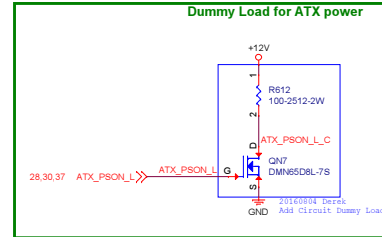
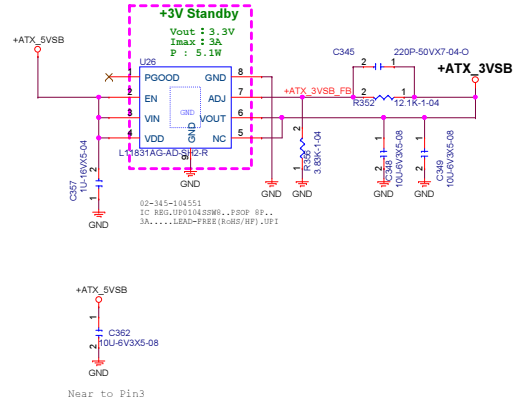
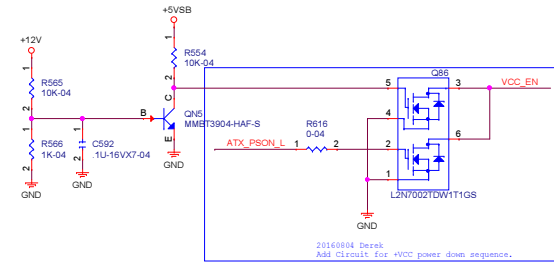
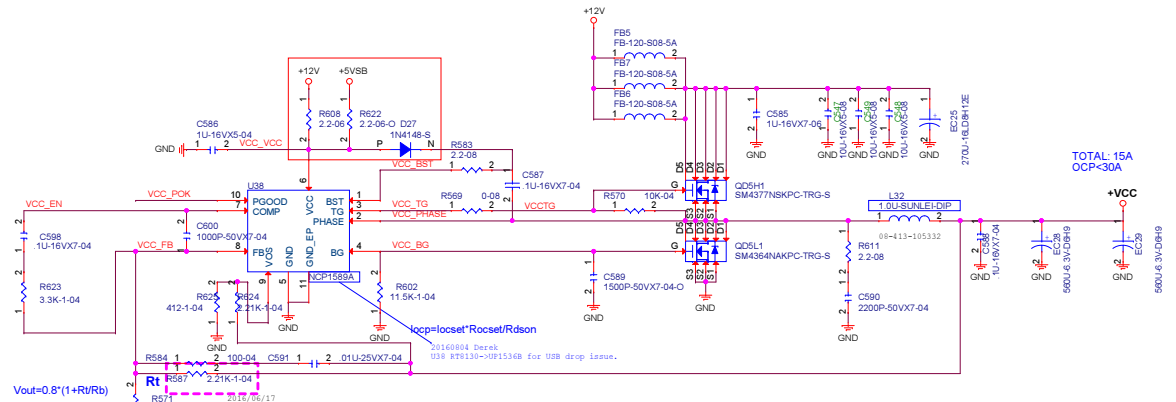
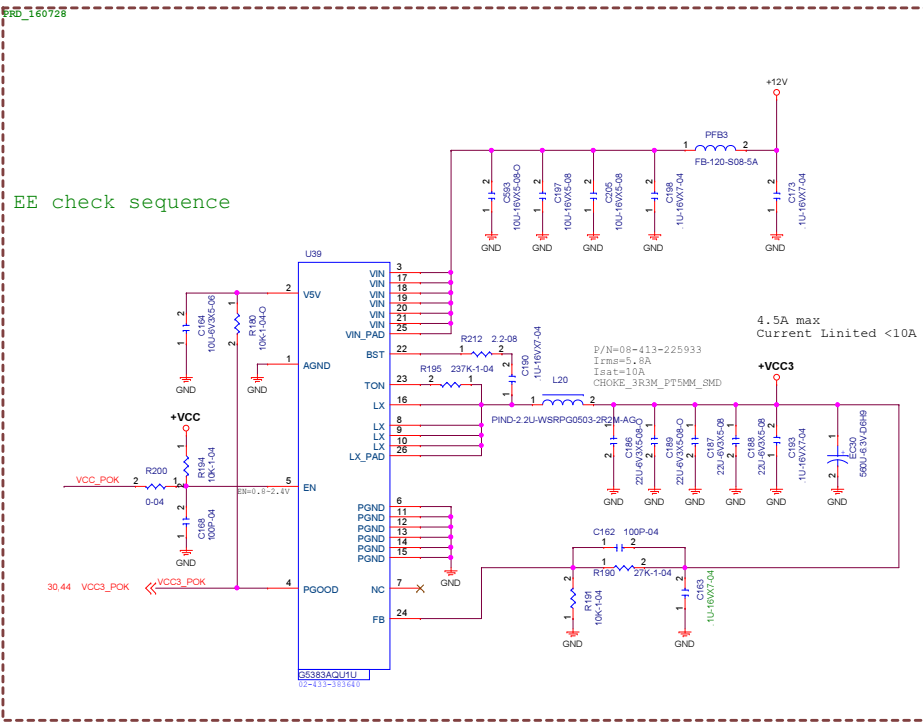
Mitch 4/7 added.

FUNCTION TABLE

INPUTS				OUTPUTS	
PRE	CLR	CLK	D	Q	\overline{Q}
L	H	X	X	H	L
X	L	X	X	L	H
H	H	\uparrow	H	H	L
H	H	\uparrow	L	L	H
H	H	L	X	Q_0	\overline{Q}_0



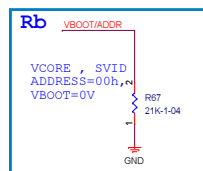
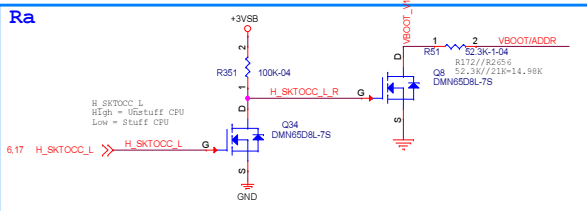
EE check sequence



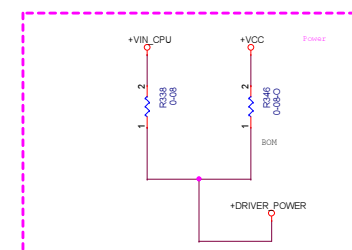
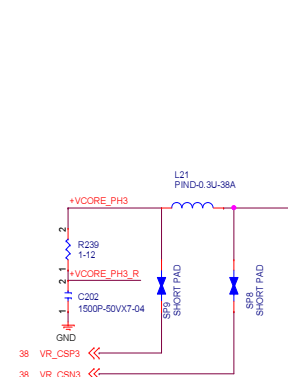
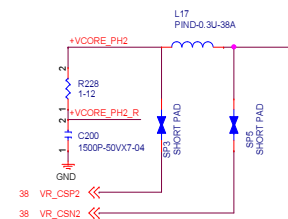
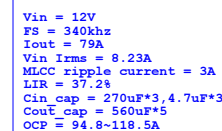
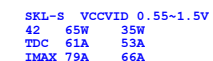
Elitegroup Computer Systems			
File	+VCC AND +VCC3		
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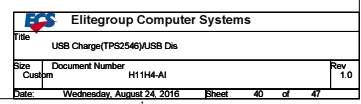
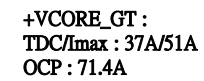
Vcore Vboot=1.2V
(stuff when sample run for testing)

FOR VCORE AND VGT VBOOT=1.05V

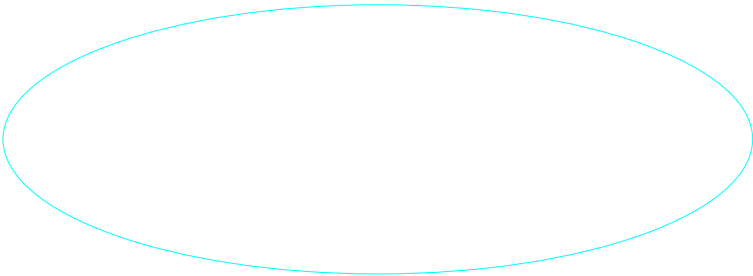
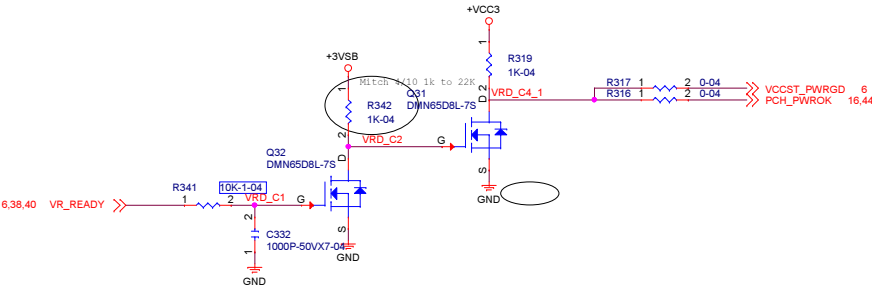


VBOOT	Ra	Rb
A3-A4	Stuff	21K-1-04
MP	Unstuff	15K-1-04

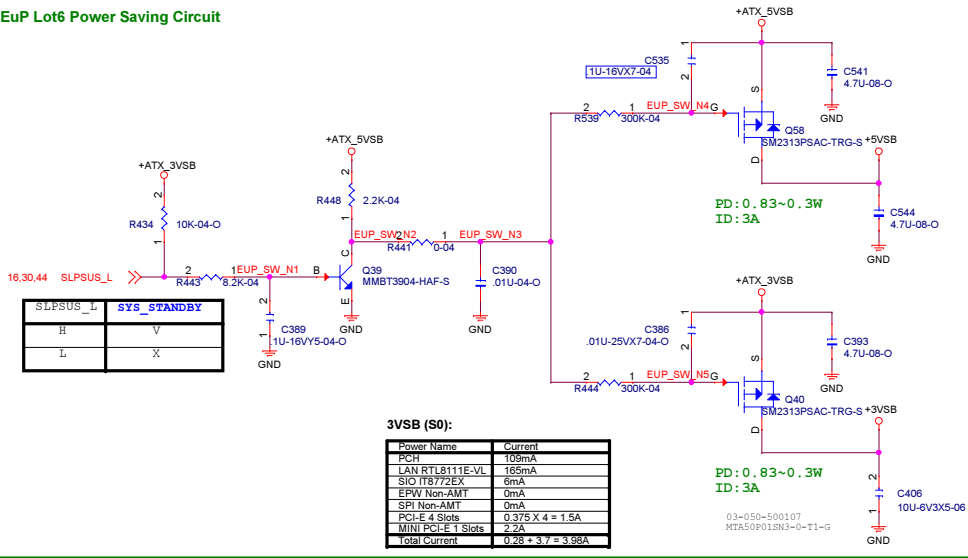




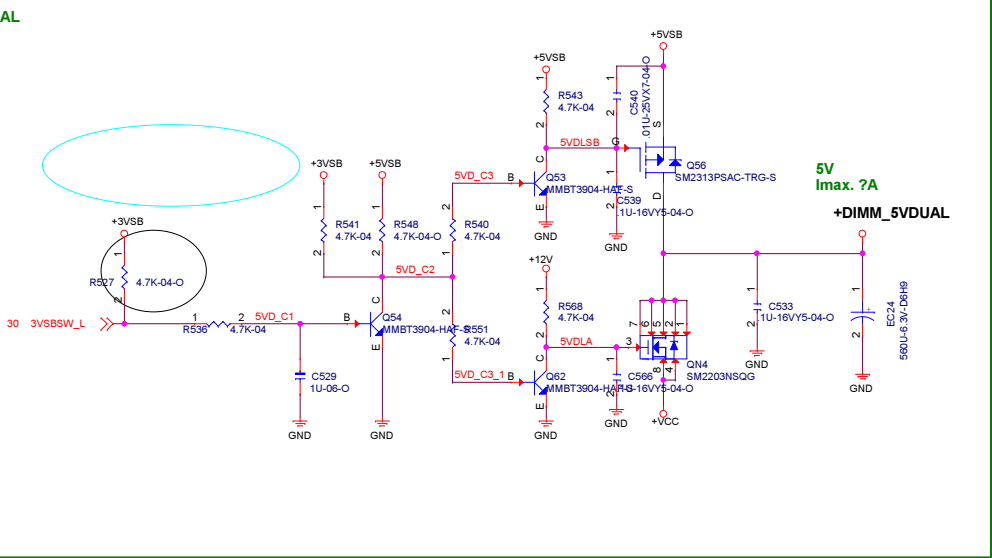
PCH & VCCST PWROK



EuP Lot6 Power Saving Circuit



5VDUAL



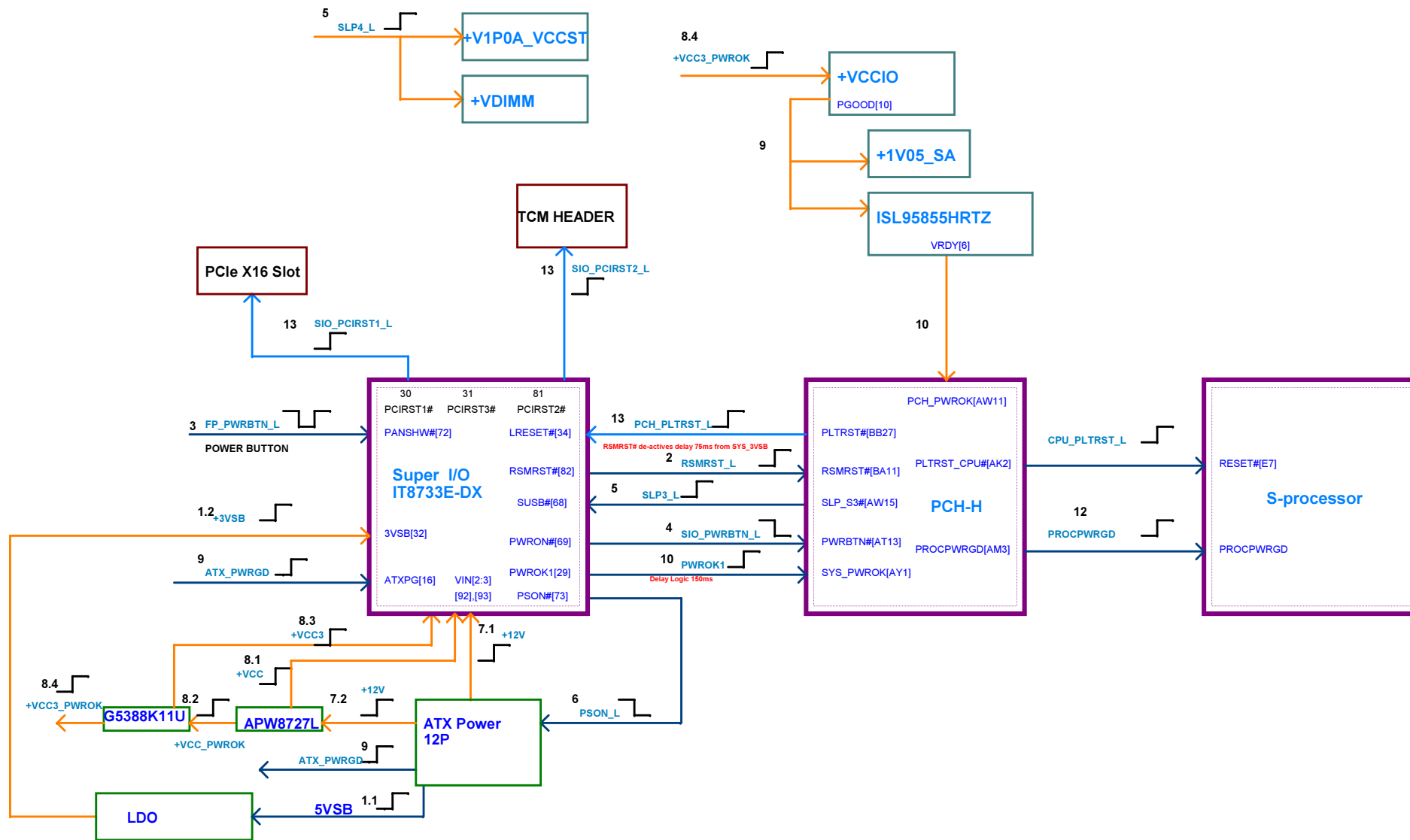


Figure 41-2. SKL S Flow Diagram for RSMRST_PWRGD# Generation

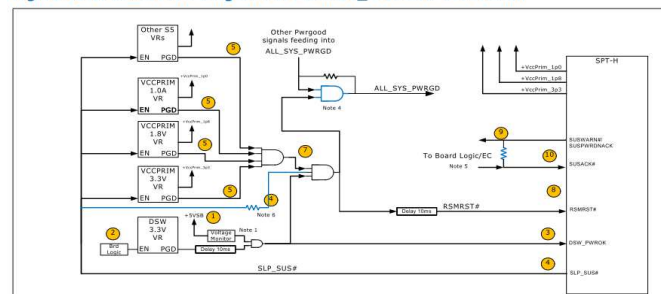
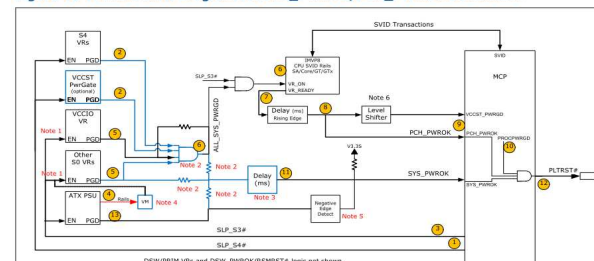


Figure 41-1. SKL S Flow Diagram for SYS_PWROK/PCH_PWROK Generation



Schematics Version History Table: Data:2014/11/28

Rev.	Date	Page	Change list	Remark
B	20160804	14	U4 01-267-166350->01-267-166351 R21 ` R22 33->0 ohm	VGA DDC Timing issue
	20160804	14	RJ3(1-2)->(2-3) Del ME_DISABLE ` R430	HW ME Disable Jumper change to SW contral.
	20160804	17	C355 1000P->150P	tCPU19 power sequence issue.
	20160804	17,31,45	C353 1000P->150P; Add C595 .1U-16VX7-04 R581 1.13K->1K; Add C570 150P R585 4.7K -> 1K-1-04; Add Q86 L2N7002TDW1T1GS Add R616 0-04 ; Add QN7 DMN65D8L-7S Add R612 100-2512-2W Add R617,R62,C594,R618,R619,Q84,Q85	tPCH14 power sequence issue.
	20160723	18	R372 56->20.5	SIO_CLKIN SI Issue.
	20160804	19	C331,C328 15P->33P	24M XTAL SI issue.
	20160723	26	EC6 100U->220U	USB2.0 Droop test
	20160804	29	C160,C161 33P->30P	24M XTAL SI issue.
	20160804	31	Add R562,R563,R564,R572,Q61,Q55	tPCH11,tPCH12 power sequence issue
	20160723	32	Power net +5VDUAL -> +DIMM_5VDUAL	Power LED issue
	20160804	38	+VCC3 power solution change G5388K11U ->G5383AQU1U	+VCC3 Power test issue
	20160804	38	+VCC power solution change APW8727L ->NCP1589A	USB drop issue
	20160728	39,40,41	R99 200K-1-04 -> 215K-1-04 R110 24.9K-1-04 -> 22K-1-04 R71/R82 30K-1-04 -> 26.1K-1-04 R117 24.9K-1-04 ->18.7K-1-04 R158 32.4K-1-04 -> 24.9K-1-04 R159 3.6K-1-04 -> 3K-1-04 R197,R196,R245,R280 2.2-08->0-08 R145 30K-1-04 -> 26.7K-1-04	VCORE,VCCGT power test
	20160728	41	C144 Add 470P-50VX7-04 R171 63.2K-1-04 ->5.9K-1-04 R169 10-04 -> 0-04	+1V05_SA power test
	201608728	42	R253 510K-1-04 -> 330K-1-04 C274 Add 22U-6V3X5-08 C230 Add 220P-50VX7-04	+1V05_SA power test
	201608723	43	U29 L11831AG-AD-SH2-R->APL5933CKAI-TRG	+2V5_DDRVPP inrush current issue.
	201608723	43	R500 2.15K->4.3K	U29 EN voltage level issue.
	201608723	45	R483 510K-1-04 -> 430K-1-04 R483 18K-1-04 -> 19.1K-1-04	+V1P0A power test